Attorney Docket No. PD-99W028 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Vu	:	Group Art Unit 2612
Serial No. 09/821,320	:	Examiner: L. T. Nguyen
Filed: 03/29/2001	:	Date:
For: IMAGING SYSTEM	:	

AFFIDAVIT UNDER 37 C.F.R. 1.131

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We, Truc Q. Vu, Frank Calabretta, James F. Asbrock and Nhan T. Do, hereby declare that we are the inventors of the IMAGING SYSTEM disclosed and claimed in the above-identified Patent Application.

Enclosed herewith is a copy of the invention disclosure, which shows that the invention was conceived by us before June 17, 1999. We worked diligently on the invention as evidenced by our filing of a Patent Application on March 29, 2001.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Truc Q. Vu — Date

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Frank Calabretta — Date

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James F Asbrock — 11/13/04

James F. Asbrock — Date

Full Name of Inventor: Nhan T. Do
Address: 2881 Ronco Drive, San Jose, Ca 95132
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Nhan Do — 10/27/04

Nhan T. Do — Date

INVENTION DISCLOSURE

6/2/99 Def 4-7-99

Raytheon

1. TITLE OF INVENTION

Digital Imager Devices on SOS/SOI CMOS Process

2. INVENTOR(S)

Name	Payroll No.	Source Code	Loc.	Bldg.	MS	Phone	Department Head
Truc Q. Vu	F4212	248450	NB	700	C1440	(949) 759-2166	Gary Warren
Frank Calabretta	12184	248940	NB	700	B1260	(949) 759-2091	Joseph Valdez
James F. Asbrock	96265	248940	NB	700	B1260	(949) 759-2604	Joseph Valdez
Nhan T. Do	N1200	248450	NB	700	C1440	(949) 759-2007	Gary Warren

3. PROOF OF CONCEPTION

A. By whom was first description written or drawing made?	Date	Time Spent	Account Charged	Location of first description/drawing
Truc Vu	1/15/99	1 hr	ND65C15	NB-C1222F
B. To whom was invention first disclosed? Gary Warren	Date 1/15/99			

4. REDUCTION TO PRACTICE

A. Was a device embodying the invention constructed and tested or the process practiced?	Yes( ) No (X)	By Whom	Date Started	Date Completed	Time Spent
B. Account Charged - Time	Account Charged - Material	Present Location of Device			
C. Present location of documents (date signed and witnessed), including photos, drawings, and data sheets showing reduction to practice.					

Note: All evidence of conception (first drawing and first written description) and evidence of reduction to practice (device embodying the invention and test date) must be retained

5. RELATION TO GOVERNMENT CONTRACT

A. Does this invention relate to work performed under a government contract?	Yes ( ) No (X)	Contract Number and Title
B. Is invention being used on a government contract?	Yes ( ) No (X)	Contract Number and Title

6. RELATED DOCUMENTS AND DISCLOSURE(S) (BY YOU OR BY ANOTHER). PLEASE ATTACH COPY

A. Is there a publication or public presentation to the invention?	Yes ( ) No (X)	Date	Identify:
B. Are there any related invention disclosures or patent applications?	Yes ( ) No (X)	Date	Identify PD No., etc.
C. Are there any proposals or reports or other documents relating to this invention?	Yes ( ) No (X)	Date	Identify:
D. Has the invention been used, discussed, demonstrated or otherwise disclosed outside the Company (such as to a vendor or customer)?	Yes ( ) No (X)	Date	To/For Whom (Company/Person):

7. SALE

A. Has product embodying invention or made by invention been proposed, sold, or offered for sale?	Yes ( ) No (X)	Order No.	Order Date	Delivery Date	Date Offered or Proposed
B. Is product embodying invention or made by invention in a deliverable item?	Yes ( ) No (X)	Delivery Date:			

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Frank Calabretta — Inventor Signature — 2/10/99 — Date

Nhan Do — Inventor Signature — 2/10/99 — Date

Read and understood by:

John T. Collett — Witness Name — Witness Signature — 2/12/99 — Date

Emad Zawaideh — Witness Name — Witness Signature — 2/12/99 — Date

Patent Docket No.

99W028

8. SUMMARY OF THE INVENTION

A. Give a brief description of your invention, particularly pointing out what is believed to be novel (the "heart" of what is new)

A CMOS digital imager built on SOS/SOI CMOS process is described in this invention. The photodetector element is a floating body NMOS. Photo-generated current in the body of the transistor causes the potential of the body to increase thus decreases the threshold voltage of the transistor. Transistor drain current is increased due to lower threshold voltage can thus be sensed by a differential sensing circuit.

The Imager is built similar to CMOS ROM structure where 2 NMOS transistor will form one bit of data. The sensing circuit is a differential amplifier which is sensing the difference in current of the photo transistor and the reference transistor. The reference transistor is an NMOS with body tied which has no response to light. The output of the amplifier will go through an 8-bit ADC to convert the signal to digital data.

The imager can be illuminated from the top or the bottom but the bottom illumination is more efficient since the gate and metal interconnect on top prevent some light from reaching the detector region (body of the transistor). For bottom illumination, transparent substrate such as sapphire in SOS wafers or quart or glass in SOI wafers are required.

The imager using radiation hard SOS/SOI CMOS process will be radiation hard.

The imager does not require a shutter. The phototransistor does not respond to light without gate bias thus provided a natural shutting function.

Color imager can be formed using 3 element per bit for the three primary colors, red, yellow, and green. Grating can be formed on the back of the substrate to function as color filter.

The imager will be very dense and fast because of the ROM configuration. The imager can be accessed sequentially or randomly.

B. Explain purpose and advantages of your invention (what will the invention do better than done previously?)

This invention allows very dense imager to be built on the SOS/SOI CMOS process. The use of standard CMOS process will provide low cost manufacturing. This approach should be able to achieve film quality when used as digital camera. The imager using SiGe on SOS/SOI will extent the detecting wavelength to the near infrared region. The ROM-like structure of the imager will provide a very low power operation, which is competitive advantage in portable electronics application.

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9. SUMMARY OF THE INVENTION (Continued)

C. Identify the Company program or product line to which the invention applies and the expected value to the program or product line. Also, identify potential commercial applications or this invention, including automotive applications, if any.

Potential application of this invention is digital camera with billions of dollars in market size. The radiation hard feature of this invention along with the ability to function in the near infrared could have strategic application in space.

D. Identify the prior art known to you which is improved upon or displaced by your invention and state in detail, if known, the disadvantages of the closest prior art.

The existing imagers are either of CCD type or CMOS imager using diode as photo-detector. The CCD imager requires 100% yield of CCD elements which incurs high cost of manufacturing. The size of the CCD array is also limited by the charge transfer efficiency of the device. The power dissipation of CCD imager is also high. CMOS imager using diode suffers from low level of photo-current of the detector. High gain amplifier is needed which increases the size and cost of the device.

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Farid Salahuddin Inventor Signature	2/10/99 Date	Hieu Do Inventor Signature	2/10/99 Date

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10. DETAILED DESCRIPTION (describe your invention in detail, using necessary additional sheets)

A. Be sure that each sheet is dated and signed by each inventor and two witnesses.

B. Attach copies of drawings or detailed reports helpful in understanding how your invention works.

C. If your invention has been tested, briefly summarize the test results which confirm the functions and advantages listed in 9B above.

The drain current of NMOS SOS/SOI device is shown in Fig.1. Curve 1 shows the characteristic of the device with body tied to source. Curve 2 with body floated and dark, and Curve 3 with body floated and under illumination. The drain current increases with illumination can be as high as tens of percent when the drain voltage is below the voltage that cause the kink in the current characteristic of a floating device. This change in current due to illumination can easily be detected by using a differential amplifier configuration.

Fig. 2 shows the schematic of one such differential amplifier. The photo imager has a ROM architecture with the modified sensed amplifier in Fig.2. The schematic of the whole imager is shown in Fig.3

In operation, each bit of data is accessed using the word and bit lines. The device being accessed are turned on by applying voltages to the gates of the two transistors. Photo-generated current begins to charge up the body of the transistor thus increases the output current. After accessing, the transistors are turned off thus no longer response to light. This feature allows the imager to operate without the need to use any shutter as in the case of CCD imager. Calibration on a pixel by pixel basis can be performed prior to displaying data by adding or subtracting a correction factor that is stored in a memory.

The imager is processed using any standard CMOS on silicon on sapphire (SOS) or silicon on insulator (SOI) wafers. The SOI wafer can be either glass or quartz formed by wafer bonding techniques. After the imager is built, the backside of the wafer will be polished to a predetermined thickness. The color filter can be integrated by:

1) Sputter metal on to the backside and use lithography to open a window for light detection.
2) Etch a grating inside the transparent window to diffract different color light to different angle. A plastic grating film can also be used by bonding it to the backside of the wafers. It is desirable to use a slanted grating to increase the diffraction efficiency of the light to the first order. Fig.4 shows the processing steps to form color filter.

The color filter can also be formed using dyed polymer materials. The integration is performed as follows:

3) Coat the back of the finished SOS-CMOS wafer with a layer of polymer which has been dyed with red color dye. Polyimide is one of such polymer.
4) Protect the area that cover the transistors which were dedicated to the red color using photolithography. Etch the rest of the film away using reactive ion etching technique.

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5) Coat the back of the wafer with a layer of spin-on-glass to be used as stop etch layer.
6) Coat the back of the wafer with a layer of polymer which has been dyed with yellow color dye. Repeat step 4 and 5 to define the yellow color detectors.
7) Coat the back of the wafer with a layer of polymer which has been dyed with blue color dye. Repeat step 4 to define the blue color detector.

Fig.5 shows the final structure of steps 3 to 7.

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99W028

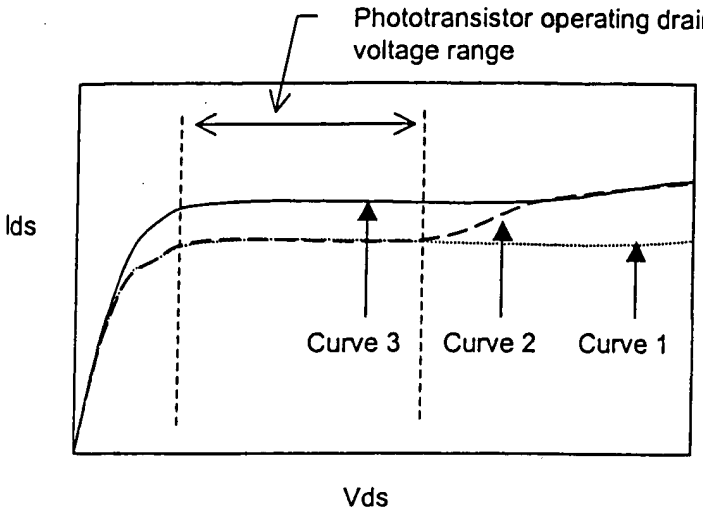

Fig.1 Drain current of an SOS/SOI NMOS with Vgs at high

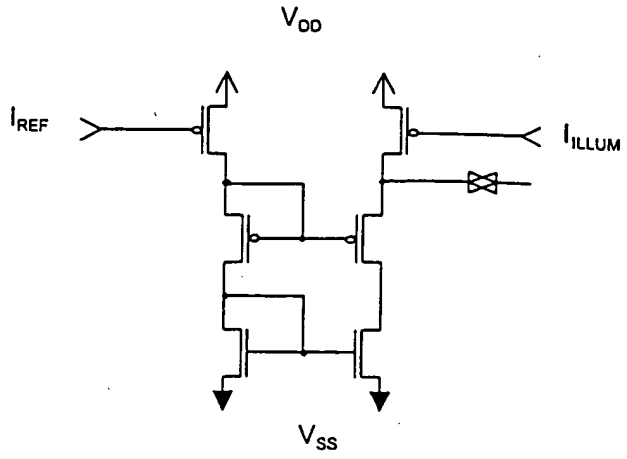

Fig. 2 Current Sense Differential Amplifier

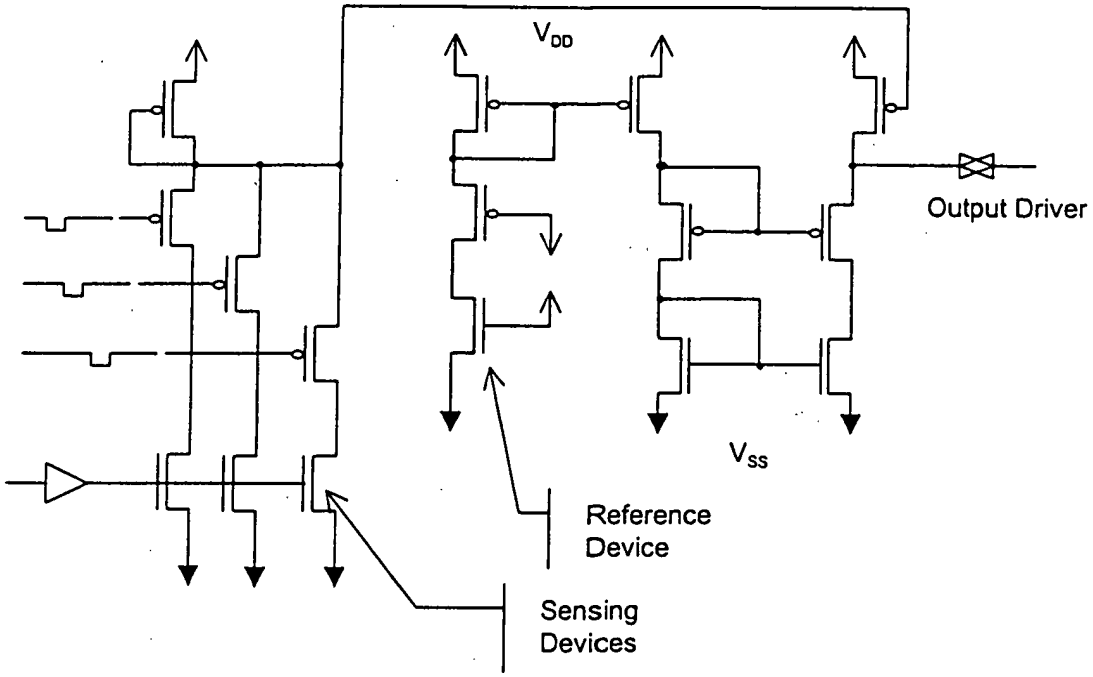

Fig. 3 Schematic illustration of a Digital SOS/SOI Imager

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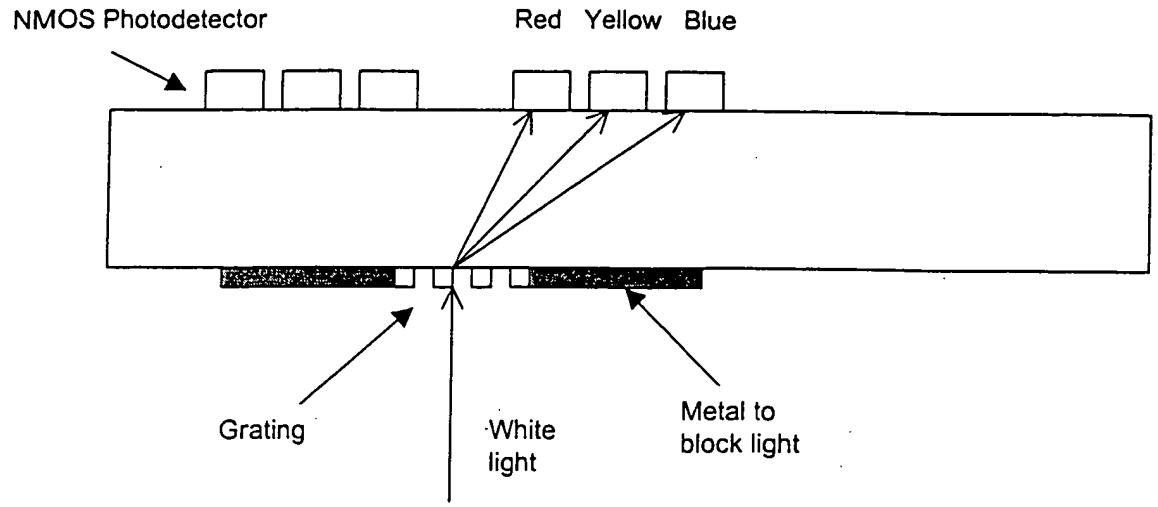

Fig.4 Structure of Color Filter using Grating

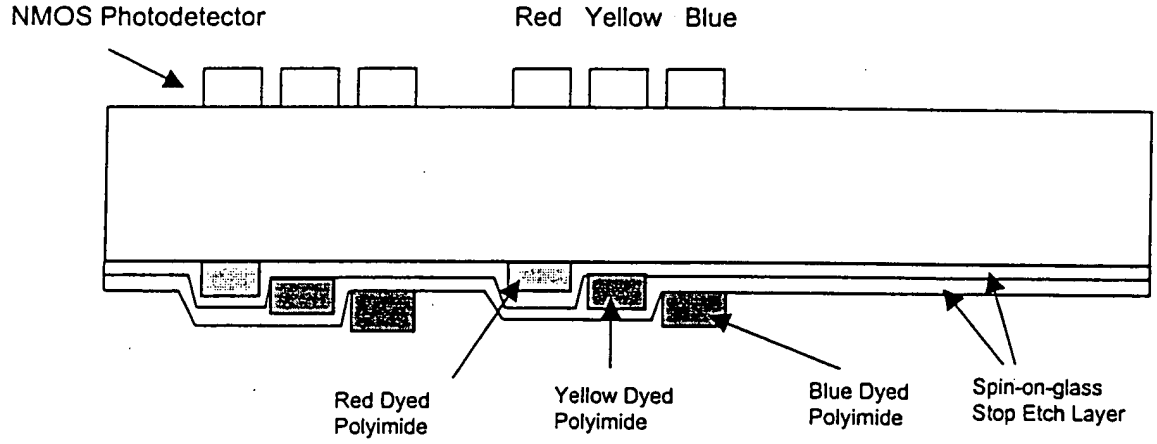

Fig.5- Structure of Color Filter using Coloring Film

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